CMOS Image Sensors With Multi-Bucket Pixels for Computational Photography

Gordon Wan, *Graduate Student Member, IEEE*, Xiangli Li, *Member, IEEE*, Gennadiy Agranov, *Member, IEEE*, Marc Levoy, *Member, IEEE*, and Mark Horowitz, *Fellow, IEEE*

***Abstract*—This paper presents new image sensors with multi-bucket pixels that enable time-multiplexed exposure, an alternative imaging approach. This approach deals nicely with scene motion, and greatly improves high dynamic range imaging, structured light illumination, motion corrected photography, etc. To implement an in-pixel memory or a bucket, the new image sensors incorporate the virtual phase CCD concept into a standard 4-transistor CMOS imager pixel. This design allows us to create a multi-bucket pixel which is compact, scalable, and supports true correlated double sampling to cancel kTC noise. Two image sensors with dual and quad-bucket pixels have been designed and fabricated. The dual-bucket sensor consists of a $640_{\mathrm{H}} \times 576_{\mathrm{V}}$ array of 5.0 μm pixel in 0.11 μm CMOS technology while the quad-bucket sensor comprises $640_{\mathrm{H}} \times 512_{\mathrm{V}}$ array of 5.6 μm pixel in 0.13 μm CMOS technology. Some computational photography applications were implemented using the two sensors to demonstrate their values in eliminating artifacts that currently plague computational photography.**

***Index Terms*—CMOS image sensor, computational photography, multi-bucket pixel, time-multiplexed exposure, virtual phase CCD.**

I. Introduction

COMPUTING rather than taking a picture is changing the requirements for image sensors. To enable low power computational features, some pixels are starting to include analog memory. A single memory enables a global shutter [1]. Adding an additional analog memory enables many more applications such as high-dynamic range imaging [2] without motion artifacts, and detection of amplitude modulated light [3], including time-of-flight 3D imaging [4]. Fig. 1 shows a conceptual view of a pixel with multiple analog memories which we call a multi-bucket pixel.

The operation of an image sensor with multi-bucket pixels is different from that of a conventional sensor. Whereas frames are acquired sequentially in a conventional sensor, in a multi-bucket sensor photo-generated charges in a photodiode can be transferred and accumulated in the in-pixel memories in any chosen time sequence during an exposure so that multiple frames can be acquired virtually simultaneously. This alternative imaging approach, called time-multiplexed exposure, eases the subsequent reconstruction algorithms in multi-image computational photography and therefore eliminates many artifacts that currently plague applications like flash/no-flash imaging [5], high dynamic range imaging using multiple exposures [2], color imaging without using a color filter array [6], and multi-flash imaging [7].

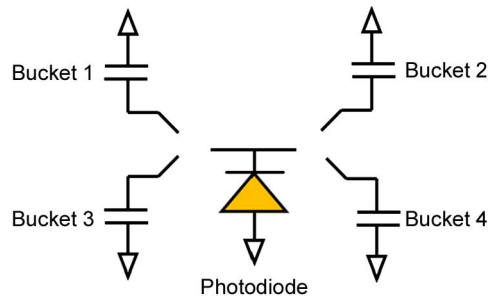

Fig. 1. A conceptual view of a multi-bucket pixel.

Designing a multi-bucket pixel which is compact and scalable is challenging because space is required to accommodate the additional in-pixel memories and their associated control signal lines. To reduce these overheads, we implemented a multi-bucket pixel by adapting the concept of virtual phase CCD [8] into a standard 4-transistor CMOS pixel such that area overhead is small and true correlated double sampling is preserved to cancel kTC noise [9].

This paper provides a more comprehensive discussion of CMOS image sensors with multi-bucket pixels. In addition to the dual-bucket sensor presented in [9], we report here on a next-generation quad-bucket sensor which comprises $640_{\mathrm{H}} \times 512_{\mathrm{V}}$ array of 5.6 μm pixel in 0.13 μm CMOS technology and new applications enabled by the sensor. We begin with a brief overview of computational photography and limitations imposed by conventional image sensors, and then follow that by a discussion of how time-multiplexed exposure, enabled by a multi-bucket sensor, can help overcome some of these challenges. In Section III, we describe a device structure which forms the basis of our multi-bucket pixels. The design and operation of two prototype multi-bucket sensors are presented in Section IV. In Section V, we present characterization results and applications of our multi-bucket sensors.

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G. Wan is with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA, and also with Aptina LLC, San Jose, CA 95134 USA (e-mail: cwan@stanford.edu).

X. Li and G. Agranov are with Aptina LLC, San Jose, CA 95134 USA.

M. Levoy is with the Department of Computer Science, Stanford University, Stanford, CA 94305 USA.

M. Horowitz is with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA.

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Fig. 2. Ghosting artifact due to motion in multiple exposure HDR photography [24]. (Online version is in color).

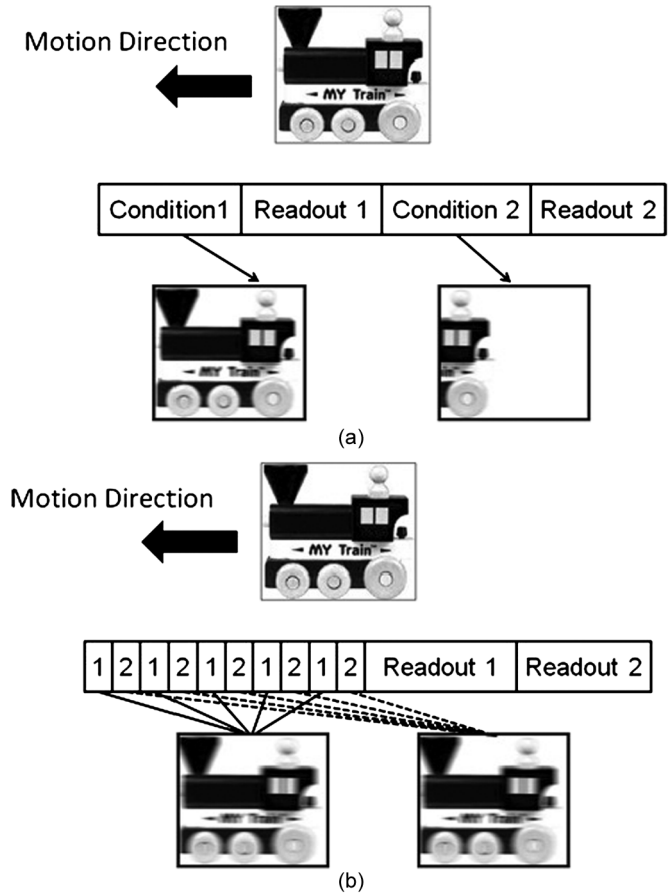

Fig. 3. Capturing two images under two conditions using (a) conventional and (b) time-multiplexed exposures.

II. Background

A. Computational Photography Using Burst of Images

Image sensors today are amazing in terms of pixel count, sensitivity, low-cost, and read noise. During this continual sensor improvement, a new approach to create images called computational photography has emerged [10], [11]. In this approach, a picture is no longer taken but rather computed from image sensor data. This added computation is performed to improve image quality or produce pictures that could not have been taken by traditional cameras. Some representative computational photography techniques include multiple exposure high dynamic range (HDR) [2], flash/no-flash [5] multi-flash [7], and panorama. A common motif to a number of computational photography techniques takes the form: "Capture a burst of images varying camera setting X and combine them to produce a single image that exhibits better Y [12]." Nevertheless, only a few photographic situations currently lend themselves to this solution because undesired changes other than setting X, such as motion, usually occur in real scenes—people walk, breezes blow, foliage moves, and hands shake [12]. Such unpredictable changes between exposures usually cause the subsequent reconstruction algorithms to fail and therefore artifacts to appear in the final computed image [13]. For example, Fig. 2 shows motion artifacts in the final picture when the objects in the scene move during the burst of images captured for a multiple exposure HDR photograph.

An ideal way to solve the problem seems to be capturing the multiple images simultaneously. However, achieving such simultaneity is impossible in a single camera system that uses a conventional image sensor because the sensor can only acquire frames sequentially. On the other hand, capturing multiple images simultaneously is not compatible with some multi-image computational photography techniques such as flash/no-flash imaging [5] in which the scene needs to be modified sequentially. In the next section, we describe an alternative imaging approach called time-multiplexed exposure that addresses this problem.

B. Time-Multiplexed Exposure

Fig. 3 shows an example of using conventional versus time multiplexed exposures to capture two images under different conditions. While the two images are captured sequentially in conventional exposure, they are partitioned into pieces and interlaced in a desirable way in time-multiplexed exposure. As shown in Fig. 3, the images corresponding to condition 1 and 2 are the sum of the sub-images captured in their respective time slots. Since the two exposures are tightly interleaved and represent the same span of time, undesired changes in the scene, such as motion in this example, are evenly distributed between

the two images. Although the time span of each image is lengthened and therefore moving objects would potentially appear more blurry (Fig. 3(b)), this interleaving eliminates the need for post-capture image alignments which are error-prone and therefore avoids reconstruction artifacts in the final image.

C. Implementation Challenges

Time-multiplexed exposure requires intermediate sub-images to be captured and accumulated inside a pixel which therefore requires pixels to have two or more analog memories. Pixels in conventional image sensors, however, are either memory-less (rolling shutter pixel) or have only one memory (global shutter pixel) [1] and therefore they do not support time-multiplexed exposure. Nevertheless, pixels with multiple memories do exist in the literature for special applications. For example, pixels with two memories, commonly known as lock-in pixels, have been used to detect amplitude modulated light [3], including time-of-flight 3D imaging [4], HDR imaging, motion detection [14], etc. Typical implementations of a pixel memory include a floating diffusion (FD) [3], [4], a MOS capacitor [15], and most recently a pinned photodiode (PPD) [14]. However, pixels reported to date have large sizes, low fill factors, high kTC noise, and cannot be easily scaled to include multiple memories.

Correlated double sampling (CDS) is the most commonly used technique to eliminate kTC noise which contributes significantly to a sensor's noise floor [1]. Fig. 4 shows a circuit schematic of a conventional 4-transistor pixel and its readout timing diagram to illustrate the CDS operation. At the beginning of the pixel readout, the FD is first reset to a high potential by turning on the reset (RST) transistor. After the FD is reset, the RST transistor is turned off. Similar to any switched-capacitor circuit, at that moment thermal noise of the RST transistor appears at the FD [16] resulting in a noise charge ($\mathrm{Q_{noise}}$) with noise power given by $\mathrm{kTC_{FD}}$ where k is the Boltzmann's constant, T is the absolute temperature, and $\mathrm{C_{FD}}$ is the floating diffusion capacitance. Since $\mathrm{Q_{noise}}$ is a random variable that varies from pixel to pixel, this reset noise or so-called kTC noise, contributes to the sensor's noise floor. In CDS, this reset level is readout through the source follower (SF) and row select (ROW) transistors biased by a current source $\mathrm{I_{bias}}$ and sampled to an external capacitor through asserting the signal SHR. Next, TX is turned on to completely transfer the charges accumulated in the PPD to the FD. This signal charge ($\mathrm{Q_{signal}}$) causes an additional drop in the FD potential. This signal level is readout and sampled to another external capacitor by asserting the signal SHS. The true signal that represents the accumulated charge in the PPD can therefore be obtained by subtracting the two sampled signals regardless of the fluctuating reset levels across the imager array [1].

To perform CDS, the charge accumulation region must be isolated from the sensing node FD or else the accumulated charges are erased when the FD is reset. Therefore, as shown in Fig. 5(a), if FD is used as a memory [3], [4], CDS cannot be performed to cancel kTC noise. Also, a separate readout circuitry is required for each memory and shared pixel architecture in which multiple neighboring pixels share the same FD and readout circuitry [1] cannot be used to minimize pixel size. Using a PPD as a memory [14] as shown in Fig. 5(b) does not suffer from the above limitations but additional signal line and gate are required for each memory added therefore causing reduction in fill factor and scalability issue. A multi-bucket pixel which is compact, scalable, and preserves true CDS to cancel kTC noise simultaneously is described next and requires a fundamentally different pixel design.

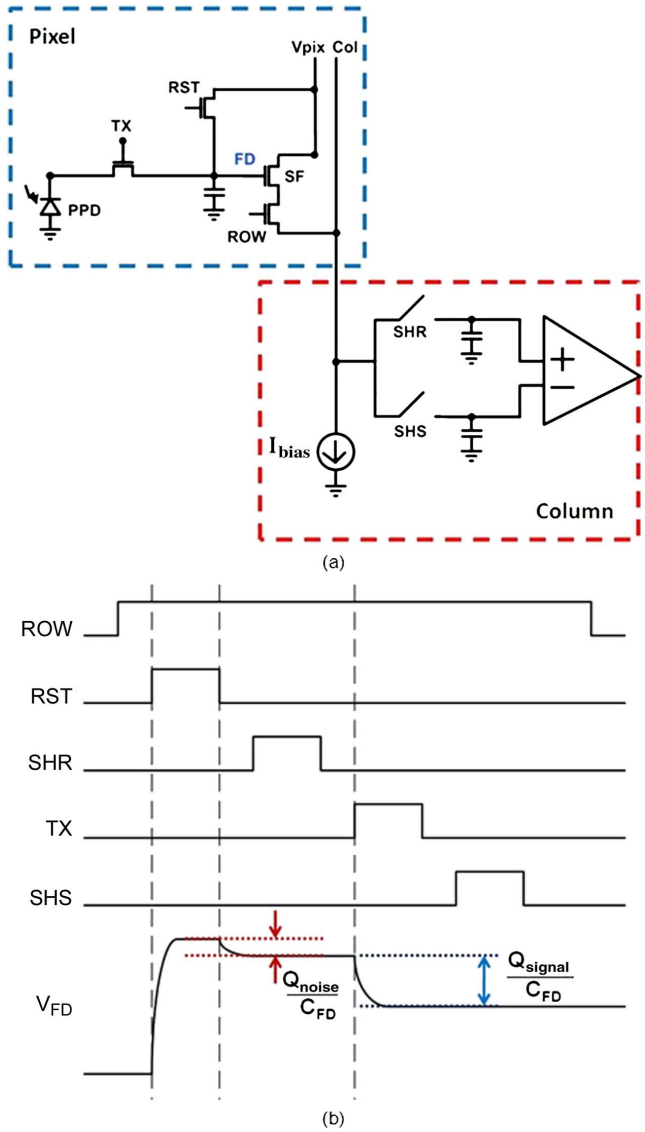

Fig. 4. (a) Circuit schematic of a 4-transistor CMOS imager pixel. (b) Readout timing diagram. The drains of RST and ROW transistors are connected to the pixel power supply (Vpix). The source of the ROW transistor is connected to the column line (Col).

III. Multi-Bucket Pixel Design

In this work, we have adapted the concept of Virtual Phase CCD (VPCCD) [8] into a standard 4-transistor CMOS imager pixel to create a class of multi-bucket pixel which is compact, scalable and preserves CDS to cancel kTC noise. Fig. 6 shows a device structure which forms the basis of our multi-bucket pixels. This proposed structure is non-standard and requires a custom fabrication process. Particularly, the structure consists

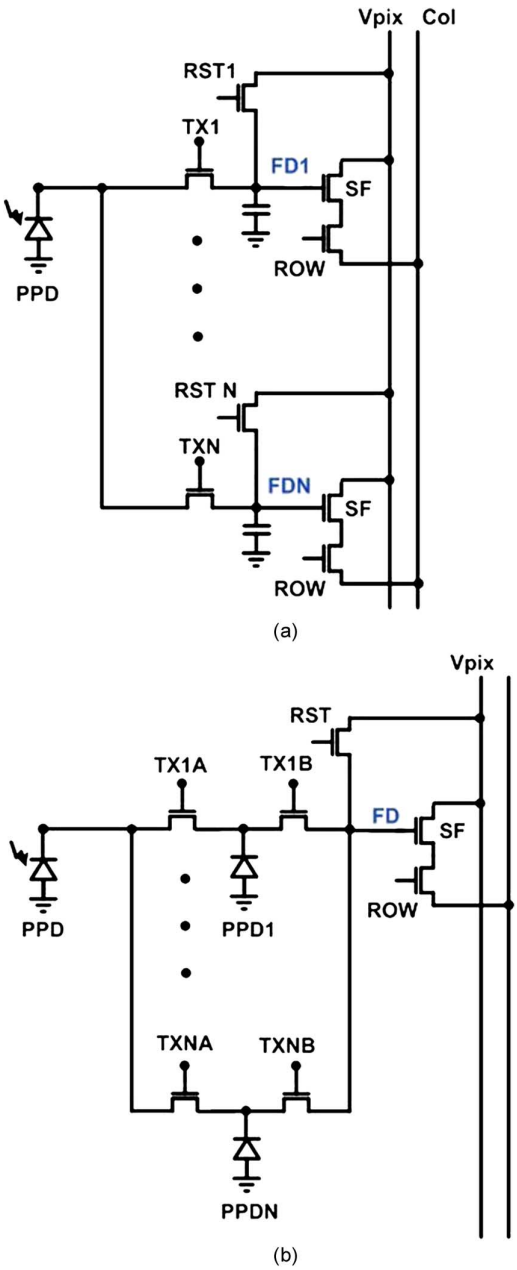

Fig. 5. Multi-bucket pixels using (a) FDs and (b) PPDs as in-pixel memories.

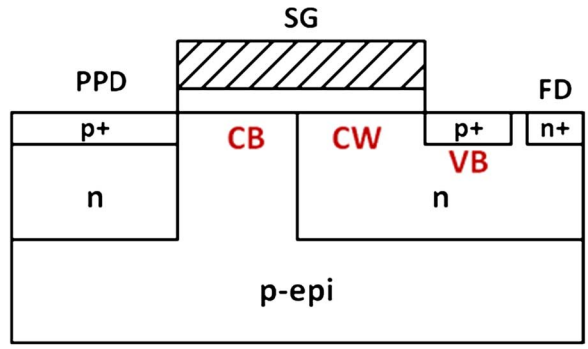

Fig. 6. Proposed device structure.

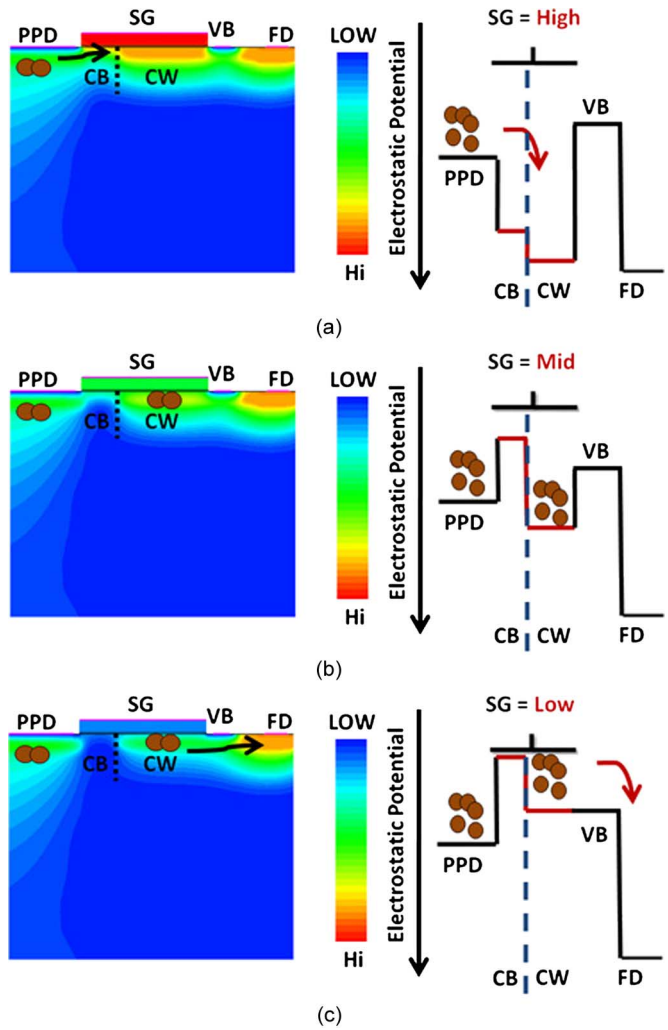

Fig. 7. Operation of the proposed device structure. The figures on the left show 2D electrostatic potentials while the figures on the right show maximum potentials inside the silicon. (a) A high voltage is applied to the SG to transfer electrons from the PPD to the CW. (b) A mid voltage is applied to the SG to store electrons under the CW. (c) A low voltage is applied to the SG to transfer electrons from the CW to the FD over the VB. (Online version is in color).

of a storage gate (SG) and a virtual barrier (VB) located between a pinned-photodiode (PPD) and a floating diffusion (FD). Similar to a VPCCD, a clocked barrier (CB) and a clocked well (CW) are formed under the SG by an additional n-type implant at the CW region while the VB region is formed by receiving one more surface p^+ implant which can be the same one used to form the PPD. These implants fix the potential of the VB and make the potential at the CW permanently higher than that of the CB. The potentials of CB and CW can be raised and lowered by application of appropriate voltages on the SG [8].

By clocking the SG with tri-level voltages, the SG and VB are used as both transfer and storage device. The key challenge is get the doping correct to create the needed potential barriers for the electrons in the silicon. Fig. 7 shows 2D electrostatic potentials and maximum potentials [17] in the silicon under different SG voltages. When a high voltage is applied to the SG, potentials at CB and CW become higher than that of the PPD causing electrons to flow from the PPD to the CW. The potential at the VB is lower than that of the CW and it prevents electrons from further flowing to the FD. When a mid-level voltage is applied to the SG, the potential at the CW is higher than those at the

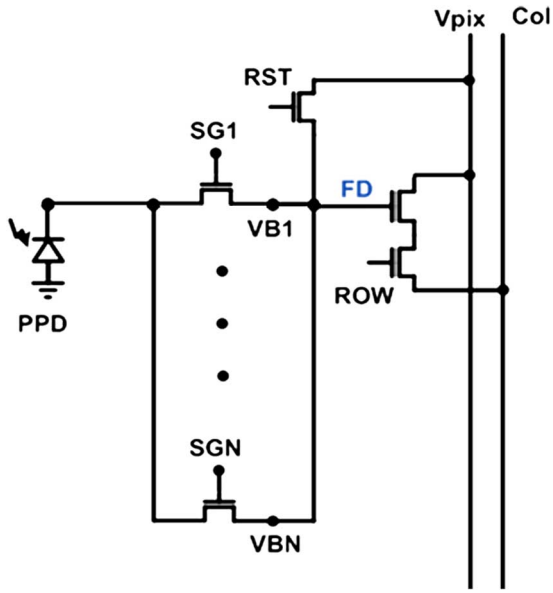

Fig. 8. A multi-bucket pixel using the proposed device as an in-pixel memory.

CB and VB and therefore electrons previous transferred from the PPD are hold in the CW. The CW thus serves as an in-pixel memory. Because of the isolation provided by the CB in this phase, a next packet of electrons can be accumulated in the PPD without mixing with electrons being stored in the CW. Additionally, the VB that isolates the CW and the FD in this phase means that the reset level of the FD can be measured without erasing electrons being stored in the CW thus allowing true CDS to be performed. Finally, when a low voltage is applied, the potential at the CW becomes lower than that of the VB and so electrons are transferred from the CW to the FD for readout.

Fig. 8 shows a circuit schematic of a multi-bucket pixel that uses the proposed device structure. Compared with using a PPD as a memory [14], this implementation eliminates one gate and one metal routing per memory making it more compact and scalable. Additionally, the same readout circuitry can be shared by all the memories and shared pixel architecture can be used to further reduce pixel size.

IV. CMOS Image Sensors With Multi-Bucket Pixels

Based on the technology described in Section III, we have designed and fabricated two CMOS image sensors with dual and quad-bucket pixels. To the best of our knowledge, sizes of the two pixels are the smallest among similar pixels reported in the literature.

A. Dual-Bucket Image Sensor

The dual-bucket image sensor comprises a $640_{\mathrm{H}} \times 576_{\mathrm{V}}$ array of 5.0 μm pixel in 0.11 μm CMOS technology. Fig. 9 shows architecture and layout of the pixel. A vertical two-way shared architecture is used to minimize pixel size. Such a shared architecture is possible because our pixel does not use the FD as a memory. Two SGs and an anti-blooming (AB) gate are connected to a PPD. Each of the SGs and its associated VB has a similar structure as the building block described in the previous section and they serve as the two buckets of the pixel. The AB

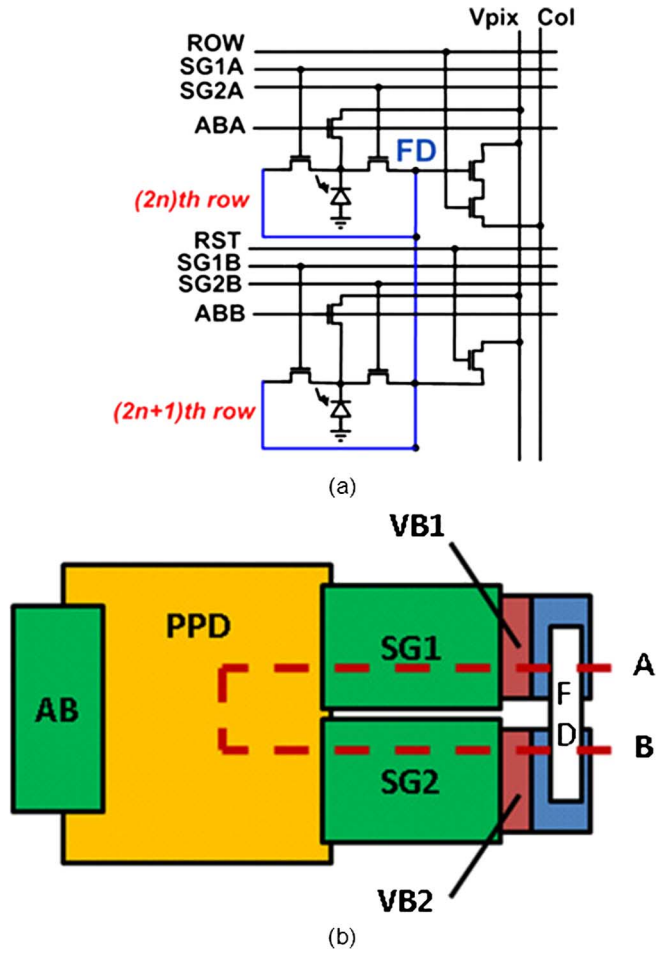

Fig. 9. The dual-bucket pixel. (a) Circuit schematic. (b) Conceptual layout.

gate is used for anti-blooming protection and resetting the PPD. Upper layer metals are routed to cover the buckets so they act as light shields to prevent parasitic light from contaminating signal charges being stored in the buckets.

Since the sensor has two buckets per pixel, it can be used to capture two time-interleaved images corresponding to two exposure conditions. Fig. 10 shows the corresponding simulations of potential profiles using Silvaco's ATHENA and ATLAS [18]. During time-multiplexed exposure, the two SGs toggle synchronously with the exposure conditions between high (e.g., 4 V) and mid-level voltages (e.g., 0.6 V–1.6 V) to transfer photo-generated electrons to the respective CWs where electrons acquired under the same condition accumulate. In each transfer, the PPD must be emptied completely or the residual electrons in the PPD would mix with the next packet of electrons acquired under a different condition in the next time slot. Therefore, the CB must be at a higher potential than the PPD when a high voltage is applied to the SG. In this case, a 4 V SG voltage is found to be sufficient to completely empty the PPD.

Compared with time-of-flight 3D imaging [4] which requires very rapid charge transfers alternatively to two storage nodes for high depth resolution, the two SGs here can toggle at a lower frequency for typical photography applications. For example, even if a short, 200 μs exposure is partitioned into 10 sub-exposures,

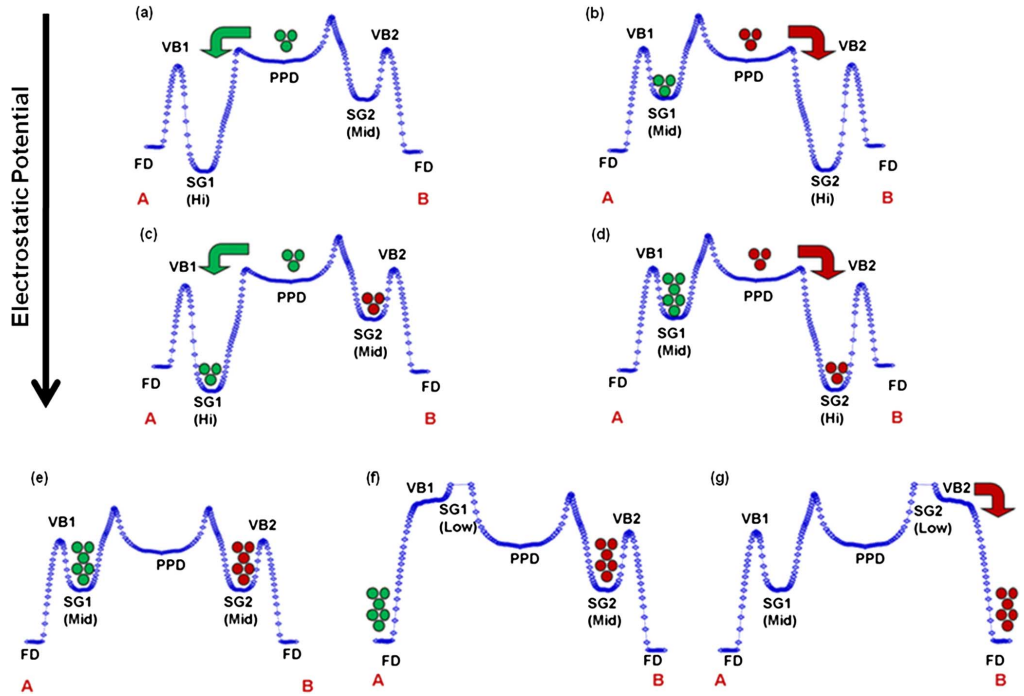

Fig. 10. TCAD simulations of potential profiles along line A-B during a time-multiplexed exposure. (a) Charge transfer from the PPD to SG1. (b) Charge transfer from the PPD to SG2. (c) Second charge transfer from the PPD to SG1. (d) Second charge transfer from the PPD to SG2. (e) Charges stored under SG1 and SG2. (f) Charge transfer from SG1 to the FD. (g) Charge transfer from SG2 to the FD.

the pulse widths of the SGs are 20 μs which is orders of magnitude longer than those required in time-of-flight applications [4].

At the end of the exposure, the same row is addressed twice to readout the signals being stored in the two SGs sequentially such that two interlaced frames are output by the sensor every frame period. In each read, the FD is reset and the reset level is sampled. The VBs that separate CWs and the FD prevent this reset action from affecting the electrons that are being stored in the CWs. To complete the true CDS operation, a low voltage (e.g., -0.5V) is applied to the SG to transfer electrons from its CW to the FD.

B. Quad-Bucket Image Sensor

To explore the design challenges of scaling up the number of buckets per pixel, and to enable computational photography techniques that require capturing more than two exposures, we have designed and fabricated a next-generation multi-bucket image sensor. This sensor has four buckets per pixel and contains an array of $640_{\mathrm{H}} \times 512_{\mathrm{V}}$ 5.6 μm pixels in 0.13 μm CMOS technology. This design doubles the number of buckets per pixel, improves pixel capacity, and maintains a similar size of the dual-bucket pixel in terms of lithographic features.

Since the quad-bucket pixel needs to accommodate two extra memories, an immediate design challenge is how pixel performance can be maintained or even improved without area overhead. Fig. 11 shows circuit schematic and conceptual layout of the pixel. Four SGs and two AB gates are connected to a PPD. Again, the AB gates serve to reset the PPD and provide anti-blooming protection. The SG and its associated VB resembles the device structure described in Section III and they serve as the four buckets of the pixel. To improve both optical and electrical symmetries, the four SGs are placed at the four corners of the PPD and they are covered by upper layer metals to protect them from parasitic light.

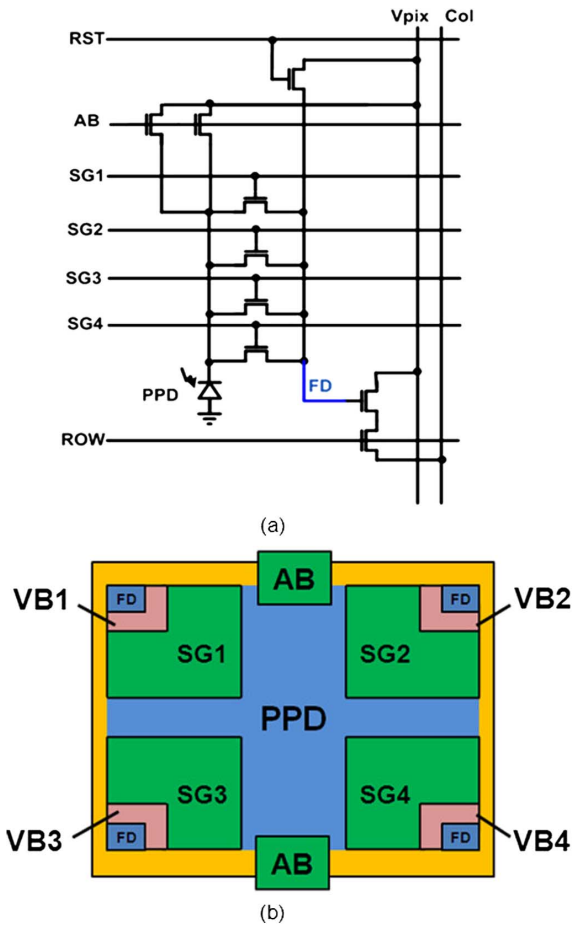

Fig. 11. The quad-bucket pixel. (a) Circuit schematic. (b) Conceptual layout.

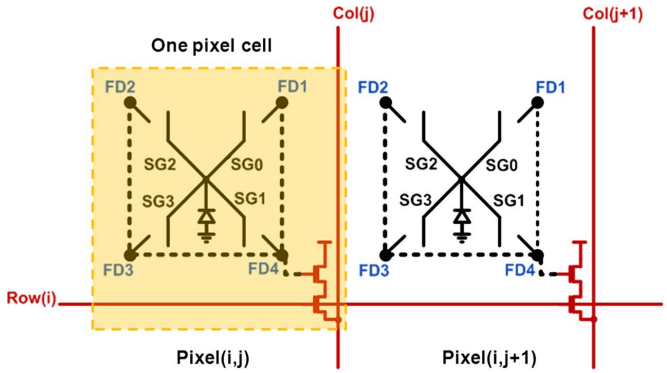

Fig. 12. Architecture of the quad-bucket pixel. The four FDs at the corners are connected and they share the same readout circuitry. The dashed lines represent metal routings connecting FDs and the gates of source followers.

Since photo-generated charges accumulate in the PPD for only a short time before being transferred to a SG during time-multiplexed exposure, from a total charge capacity perspective we can enlarge the size of each SG and reduce that of the PPD to minimize the impact of adding two extra buckets in pixel area so that pixel size is kept small, comparable to the dual-bucket pixel. Reducing the PPD size and thus the fill factor, however, causes a concern about the pixel's quantum efficiency. Fill factor, however, is only part of the many factors that determines a pixel's quantum efficiency and its impact diminishes particularly when the pixel size is large. By engineering the microlens and optimizing the optical stack, such as adding light guiding structure [19], a major portion of light falling on the pixel opening can still be guided and collected despite a smaller PPD. In this work, we simply used a standard microlens and did not attempt to optimize our light path. While this did affect our sensitivity (see Section V), even a simple microlens was able to reduce the effect of the small fill factor.

The four FDs at the corners of the pixel are electrically connected by metal and share the same readout circuitry as shown in Fig. 12. For simplicity, we represent each SG as a switch in the figure. Connecting all the FDs together in the pixel allows them to share the same readout circuitry, but lowers the pixel's conversion gain due to the parasitic capacitances of the long metal routing needed to connect FDs at the corners and device capacitances of the FD regions.

Finally, to enable a lower voltage operation, each CB is made to be at a higher potential than that of the dual-bucket pixel at the same SG bias by modifying some of the threshold adjustment implants. Therefore, a lower SG voltage is sufficient to completely empty the PPD (from 4 to 3.5 V) in the quad-bucket pixel.

Similar to that of the dual-bucket sensor, the four SGs can toggle between high (e.g., 3.5 V) and mid-level voltages (e.g., 0.6–1.2 V) during time-multiplexed exposure while a low voltage (e.g., −0.5 V) is used to readout the charges. The same row is addressed four times sequentially to readout the captured images in the four SGs using true CDS.

V. Experimental Results

Table I summarizes characteristics of the fabricated sensors and Fig. 13 shows the chip micrograph and packaged die of the sensors. The dual-bucket sensor has a higher conversion gain and therefore lower read noise compared with the quad-bucket one. The experimentally measured conversion gains match closely with our simulations using Silicon Frontline's F3D

TABLE I
Summary of Sensor Characteristics at 1.2 V SG Mid-Level Voltage

	Dual-Bucket	Quad-Bucket
General Specifications		
Pixel Size	5μm	5.6μm
Pixel Architecture	2-Way Shared	Unshared
Fill Factor	42%	10%
Resolution	640_Hx576_V	640_Hx512_V
Number of Storage Node	2	4
Shutter Type	Global Shutter	Global Shutter
Sensor Characteristics		
Conversion Gain	51uV/e	33uV/e
Storage Node Capacity	10ke	23ke
Read Noise (@Gain = 8X)	5.5e	8e
Dark Current (@Room Temperature)	20nA/cm^2	7.2nA/cm^2
Peak Quantum Efficiency	71.5%	39.5%
Responsivity (@550nm)	74ke/lux-s	49ke/lux-s
FPN (@50% Signal)	0.98%	1.10%
Temporal Noise (@50% Signal)	1.36%	0.93%

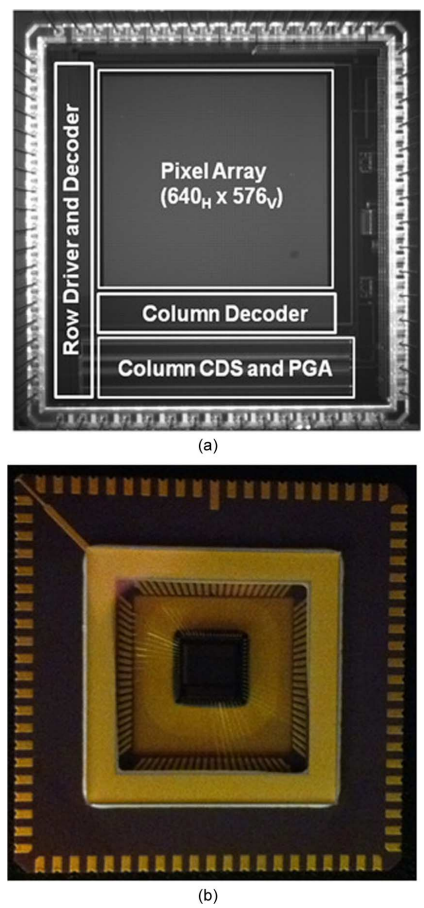

Fig. 13. (a) Chip micrograph of the dual-bucket sensor and (b) packaged die of the quad-bucket sensor.

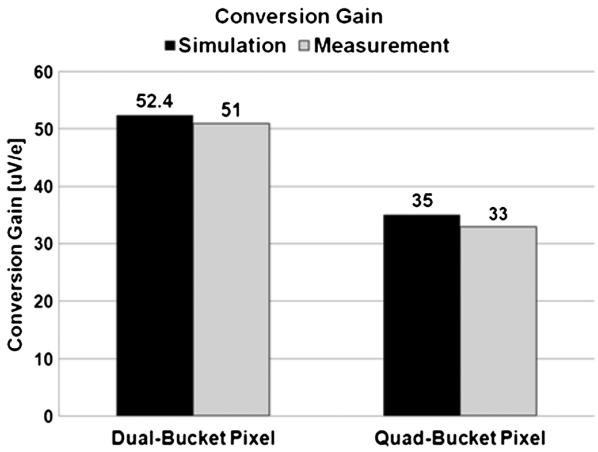

Fig. 14. Conversion gain simulation and measurement results.

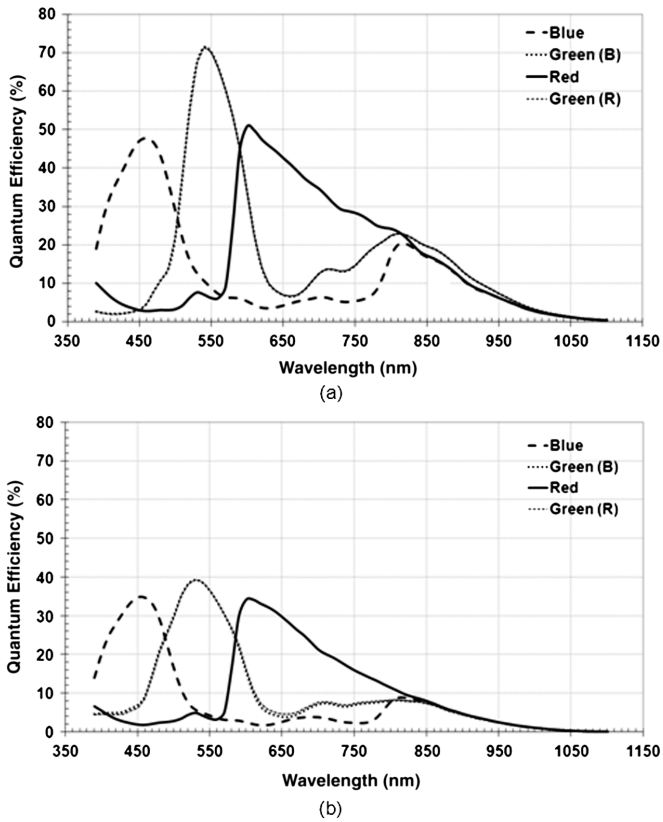

Fig. 15. Measured quantum efficiencies of (a) the dual-bucket pixel and (b) the quad-bucket pixel.

[20], [21] as shown in Fig. 14. Fig. 15 shows the measured quantum efficiencies of the two pixels. As we have predicted, even though the quad-bucket pixel has four times smaller fill factor and no optimization has been made on the microlens and light path, its quantum efficiency is decreased by less than two times from the dual-bucket pixel across visible wavelengths. This result points to the fact that microlens, even though not being optimized in the current sensors, is effective in focusing light from the pixel opening to the PPD.

On the other hand, the quad-bucket pixel does achieve more than two times improvement in storage capacity per SG under

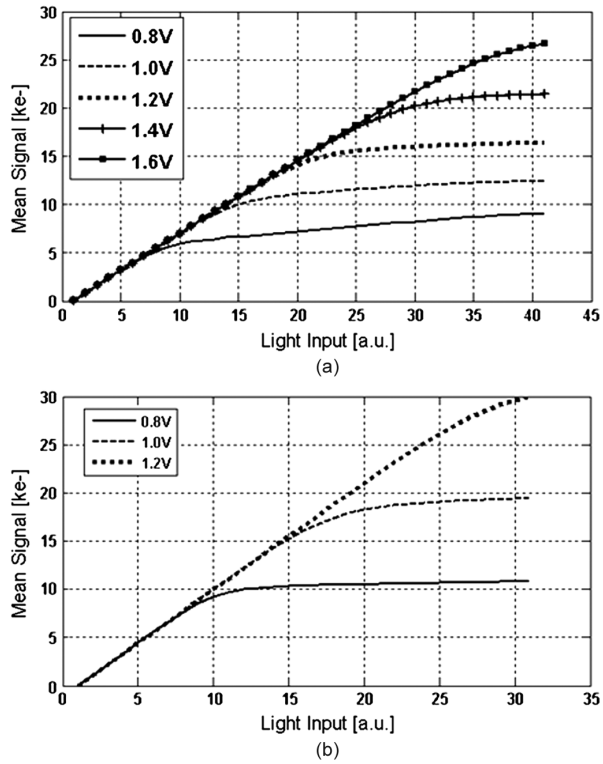

Fig. 16. Measured photo-response of (a) the dual-bucket pixel and (b) the quad-bucket pixel with respect to different SG mid-level voltages.

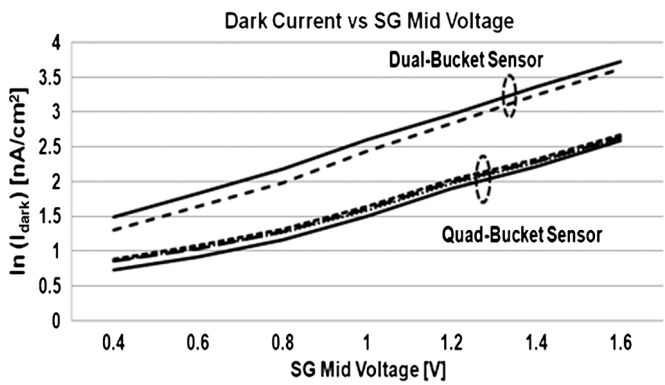

Fig. 17. Measured SG dark current at room temperature with respect to different SG mid-level voltages. The different curves represent dark currents of different SGs.

the same biasing voltage (e.g., 1.2 V). Figs. 16 and 17 show the measured photo-responses and SG dark currents at room temperature of the two pixels under different SG mid-level voltages, respectively. Storage capacity of a SG increases with increasing SG mid voltage. The operating voltage is then a trade-off between storage capacity and dark current, which also increases with increasing storage voltage. We can take advantage of this relationship to create an adaptive gate biasing scheme in which a low SG mid voltage is used under low light situation to mitigate dark current while a high SG mid voltage is used under strong light situation to maximize pixel capacity.

The remainder of this section briefly describes some simple computational photography results that are enabled by our sensors.

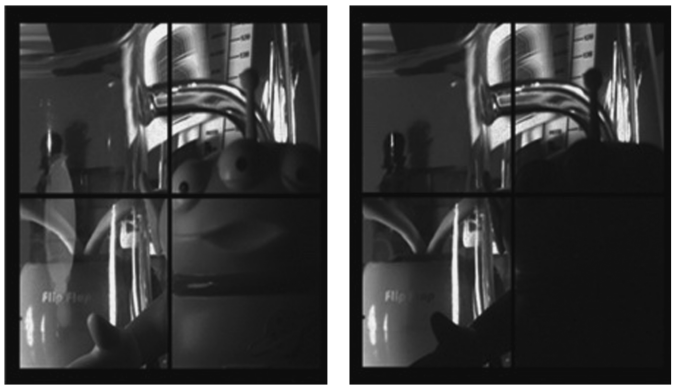

Fig. 18. Flash/no-flash imaging. The scene is illuminated by a pulsing LED flash. A toy alien and an apple are placed in front of and behind a glass beaker, respectively. The letter "S" attached on an oscillating metronome needle placed at the back shows the same motion blurs in both flash/no-flash images. (a) SG synchronized with the flash, (b) SG not synchronized with the flash. The four windows separated by black lines in the images correspond to pixels with slightly different designs.

1) Flash/No-Flash Imaging: In flash/no-flash imaging [5], a pair of flash and no-flash images is taken to synthesize an image which preserves natural ambient illumination and has dark regions of a scene correctly exposed. However, this technique has a limitation that even a slowly moving scene between the two exposures causes motion artifact [5]. The dual-bucket sensor overcomes this limitation by alternating between a LED flash and no flash and synchronizing the flash with one of the SGs. Compared with a conventional sensor, the dual-bucket sensor produces two images representing the same span of time and having roughly the same motion as demonstrated in Fig. 18. The letter "S" attached on an oscillating metronome needle has similar blurs in both flash/no-flash images.

2) HDR Imaging: Most HDR applications use multiple exposures [2], with varying exposures to capture the true dynamic range of a scene and tone map this data to synthesize a HDR image. This approach requires the scene to be relatively stationary or otherwise ghosting artifact would appear in the synthesized image [24]. Our dual-bucket sensor handles this situation by fluttering the SGs so that the two buckets are recording over the same time interval, with duty cycles of the SG clocks setting the desired exposure ratio. Since the two images are interleaved in time, error-prone image alignment is not needed when combining the images and therefore reconstruction artifact is avoided. By using four instead of two exposures, the quad-bucket sensor can span a higher dynamic range or reduce signal-to-noise ratio (SNR) dips at transition points between exposures [22]. Fig. 19 shows images captured by the quad-bucket sensor with four different exposure times, 8:4:2:1 in this example, and a synthesized HDR photograph. Even without image alignment or motion compensation, the computed image does not show motion or color artifacts. In this example, the quad-bucket sensor spans 85 dB dynamic range with 3 dB SNR dip at each transition point. A 103 dB dynamic range with 6 dB SNR dip can be achieved if the ratio between each of the four exposures is changed from 2 to 4.

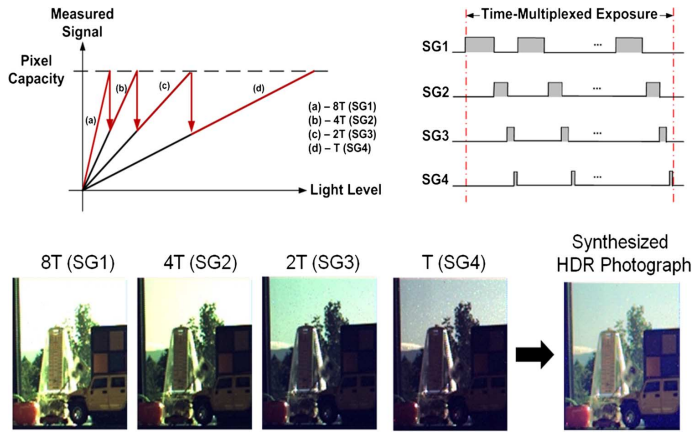

Fig. 19. Time-interleaved quad-exposure HDR photography without motion and color artifacts. (Online version is in color).

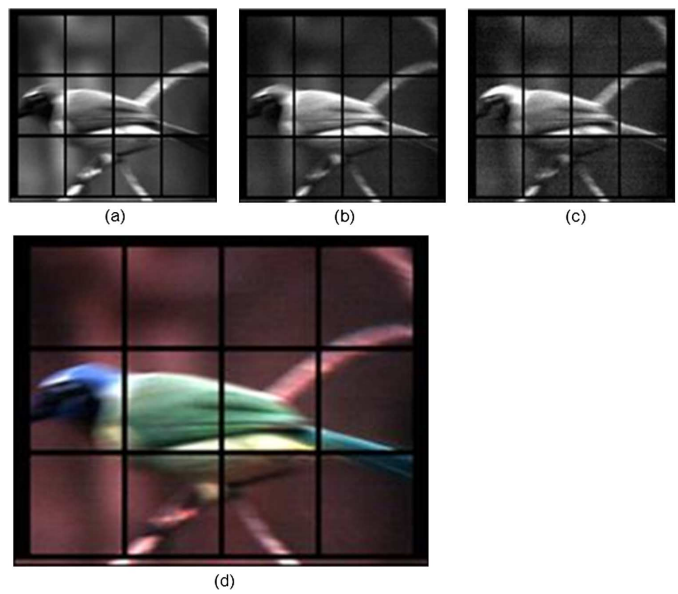

Fig. 20. CFA-less color imaging. (a) Red, (b) green, (c) blue images captured by SG1, SG2, and SG3 synchronized with R, G, and B light sources, respectively. (d) Synthesized color image. Color artifact due to motion is not observed. (Online version is in color).

3) Color Imaging Using Active Illumination: The quad-bucket sensor can be used to perform color imaging using active illumination without a color filter array (CFA) [6]. Three time-interleaved RGB light sources are used to illuminate a scene while three SGs are synchronized with the light sources. The images are then combined to form a color picture as shown in Fig. 20. Color artifacts commonly observed when a conventional sensor is used [23] are removed due to the time-interleaved nature of the captured images. Given excellent color fidelity due to the lack of cross-talk and improved light sensitivity by eliminating the CFA, this approach is attractive in light-limited applications such as capsule endoscopy [6].

4) Multi-Flash Imaging: Fig. 21 shows the experimental setup that demonstrates using the quad-bucket sensor for time-interleaved multi-flash imaging [7]. Four time-interleaved light

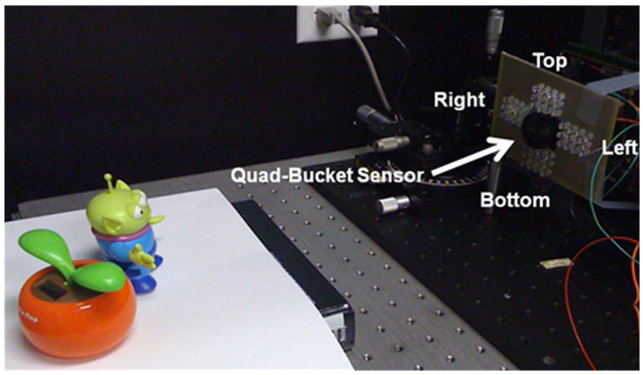

Fig. 21. Experimental setup of time-interleaved multi-flash imaging. (Online version is in color).

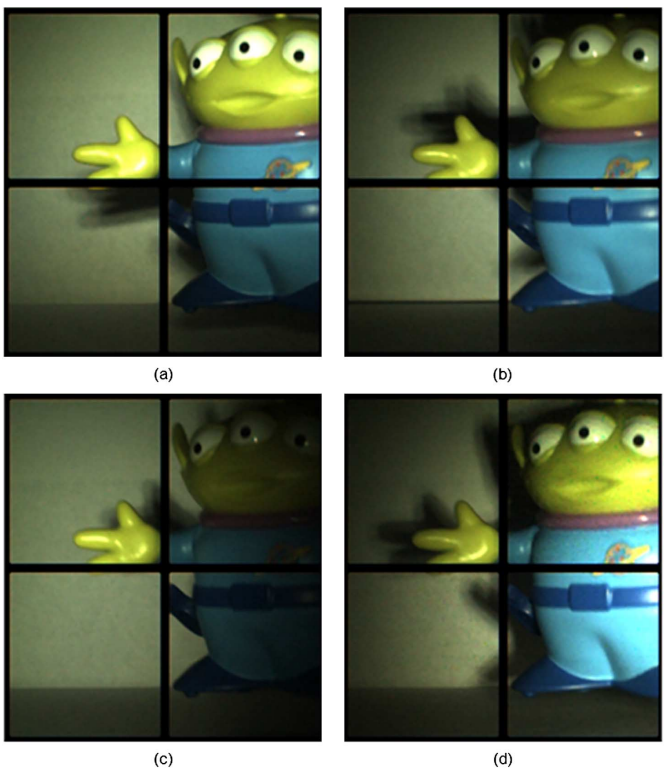

Fig. 22. Time-interleaved multi-flash imaging. Images captured when (a) top, (b) bottom, (c) left, (d) right LED groups are illuminating the scene. (Online version is in color).

sources are used to illuminate an object with each SG synchronized with one of the light sources so it captures the corresponding image as shown in Fig. 22. By computationally combining the four captured images, a shadow-free image as shown in Fig. 23 is synthesized. In contrast to a conventional sensor, the quad-bucket sensor time-interleaves the captures and makes this approach more robust to motion in the scene.

From the above applications, we can see that the multi-bucket sensors, through enabling time-multiplexed exposure, avoid many artifacts that computational photography faces when a conventional sensor is used.

Fig. 23. Synthesized shadow-free Image. (Online version is in color).

VI. Conclusion

Photography is changing, and image sensors will need to change as well. By adding analog memories in each pixel, the multi-bucket CMOS image sensors presented in this paper can tightly interleave two or four captures, allowing the user to control which light goes into which bucket. We have seen how this enables various computational photography applications such as flash/no-flash imaging, HDR imaging without motion artifacts, color imaging with active illumination, and multi-flash imaging. Since the captures are interleaved, there is no need to perform error-prone image alignments which used to be necessary to cope with undesired scene changes and therefore artifacts that plague those applications can be avoided. Future work includes further optimization of pixel performance, shrinking pixel to smaller size, and demonstrating how the sensors can enhance other computational photography applications.

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Gordon Wan (S'11) received the B.S. degree in electrical engineering and mathematics from the University of Texas at Austin, in 2005 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 2007 and 2011, respectively.

He has held intern positions at Motorola Semiconductor, Silicon Laboratories, Intersil, and Qualcomm in 2002, 2004, 2006, and 2007 respectively. Since 2009, he has been with the imaging technology group of Aptina Imaging, San Jose, CA, where he focuses on research and development of next-generation imaging pixels and algorithms. His current research interest is in imaging technology. Particularly, he is interested in developing new pixel and sensor technologies, as well as the associated software algorithms that would benefit from those technologies.

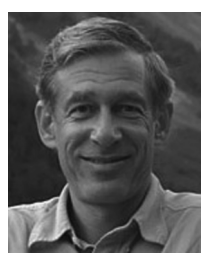
Dr. Wan was a recipient of the James F. and Mary Lynn Gibbons Fellowship, the Stanford Graduate Fellowship, and the Pan Wen Yuan Scholarship.

Xiangli Li (M'10) was born in Hebei, China, in 1973. He received the B.S. degree in electrical engineering from Nankai University, Tianjin, China, in 1996, the M.S. degree in electrical and computer engineering from University of Idaho, in 2003, and the Ph.D. degree in electrical and computer engineering from Boise State University, ID, in 2008.

In 1996 to 2001, he worked in Motorola (China) Ltd., as a Product Engineer working on first generation GSM mobile phone introduction and manufacturing. In January 2004, he joined the Micron Imaging Group as a Characterization Engineer working on CMOS image sensor electrical and optical characterization. Since 2006, he is a Design and Characterization Manager leading Aptina Pixel R&D Group working on next generation pixel development including test chip design, pixel design and characterization, pixel optical and electrical performance optimization for different applications. He holds 5 U.S. patents and 13 patents applications are pending related to CMOS image pixel/sensor design and operation.

Gennadiy Agranov (M'05) graduated in the Physics of Semiconductors from the St. Petersburg University of Electrical Engineering, Russia, in 1973 and received the Ph.D. degree from the Moscow Institute of Microelectronic Devices, Russia, in 1984, for his work on large infrared focal plane arrays for space application.

Until 1998, he was with Electron National Research Institute, St. Petersburg, developing and investigating different types of infrared focal plane arrays, CMOS readout circuits, and CCD image sensors. He also served as an Associate Professor at St. Petersburg State Technical University, from 1995–1997. He has received an academic title "Senior Researcher" from the Highest Certification Commission, Russia, in 1991. From 1992 to 1995, he was a member of the Special Council of Electronic Industry Ministry on the problem of IR-photodetectors for Space Applications. After relocation to the USA in 1999 he joined Photobit Corporation, Pasadena, CA, as a Research Scientist. He was responsible for the full characterization and optimization of most image sensors developed at Photobit. He joined Micron Technology Incorporation as a Senior Research Scientist in 2001 after the acquisition of Photobit. In 2002, he worked as a Characterization Engineering Manager and in 2004, was recognized as a Fellow. Since 2008, he is a Vice President of Imaging Technology at Aptina Imaging. His research interests include in-deep photoelectrical characterization and investigation of CMOS image sensors, optimization of optical and electrical performance of CMOS imaging devices, and pixel development for advanced image sensors. He has published 68 technical papers, received six Russian patents, and nine USA patents; more than 20 US patents are pending.



Marc Levoy (M'89) received the Bachelor's and Master's degrees in Architecture from Cornell University, Ithaca, NY, in 1976 and 1978, and the Ph.D. degree in computer science from the University of North Carolina at Chapel Hill, in 1989.

Currently, he is the VMware Founders Professor of Computer Science at Stanford University, Stanford, CA, with a joint appointment in the Department of Electrical Engineering. In the 1970s he worked on computer animation, developing a cartoon animation system that was used by Hanna-Barbera Productions to make *The Flintstones, Scooby Doo*, and other shows. In the 1980s, he worked on volume rendering, a technique for displaying three-dimensional functions such as computed tomography (CT) or magnetic resonance (MR) data. In the 1990s he worked on 3D laser scanning, culminating in the Digital Michelangelo Project, in which he and his students spent a year in Italy digitizing the statues of Michelangelo. Outside of academia, he codesigned the Google Book Scanner and launched Google's Street View project. His current interests include light fields. optical microscopy, and computational photography—meaning computational imaging techniques that extend the capabilities of digital photography.

Dr. Levoy is an ACM Fellow (2007). He received the Charles Goodwin Sands Medal for Best Undergraduate Thesis (1976), National Science Foundation Presidential Young Investigator Award (1991), and the ACM SIGGRAPH Computer Graphics Achievement Award (1996).

Mark Horowitz (F'00) received the BS and MS degrees in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, in 1978, and the Ph.D. degree from Stanford University, Stanford, CA, in 1984.

Currently, he is the Chair of the Electrical Engineering Department and the Yahoo! Founders Professor of the School of Engineering at Stanford University. His research interests are quite broad and span using EE and CS analysis methods to problems in molecular biology to creating new design methodologies for analog and digital VLSI circuits. He has worked on many processor designs, from early RISC chips to creating some of the first distributed shared memory multiprocessors, and is currently working on on-chip multiprocessor designs. Recently he has worked on a number of problems in computational photograph. In 1990, he took leave from Stanford to help start Rambus Inc., a company designing high-bandwidth memory interface technology, and has continued work in high-speed I/O at Stanford. His current research includes updating both analog and digital design methods, low energy multiprocessor designs, computational photography, and applying engineering to biology.

Dr. Horowitz is a fellow of IEEE and ACM and is a member of the National Academy of Engineering and the American Academy of Arts and Science. He has received many awards including a 1985 Presidential Young Investigator Award, the 1993 ISSCC Best Paper Award, the ISCA 2004 Most Influential Paper of 1989, the 2006 Don Pederson IEEE Technical Field Award, and the 2011 SIA Faculty Researcher Award.