DRAM Design Overview

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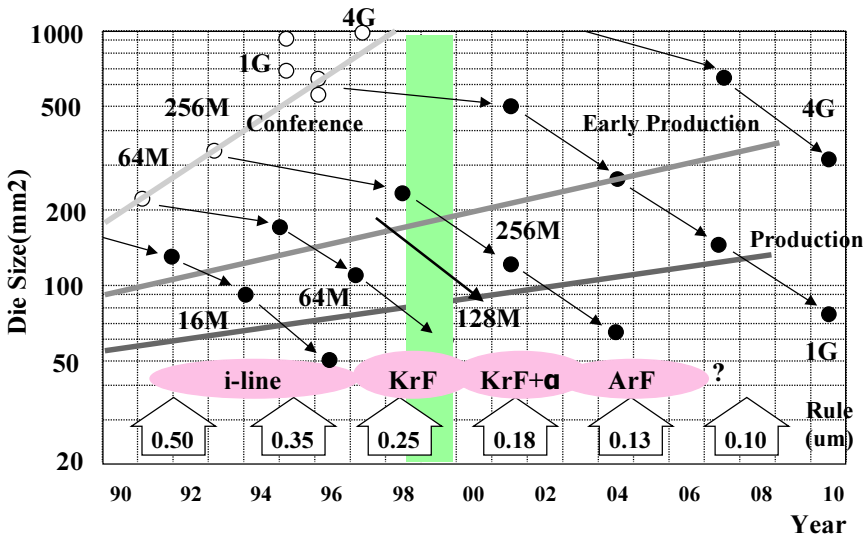
Contents

- *Trends of Standard DRAM*
- *History of DRAM Circuits*
- *Cell, Array and Major Circuits*
- *Embedded DRAM*
- *ASM Example*
- *Summary*

DRAM Design Overview

Standard DRAM Development



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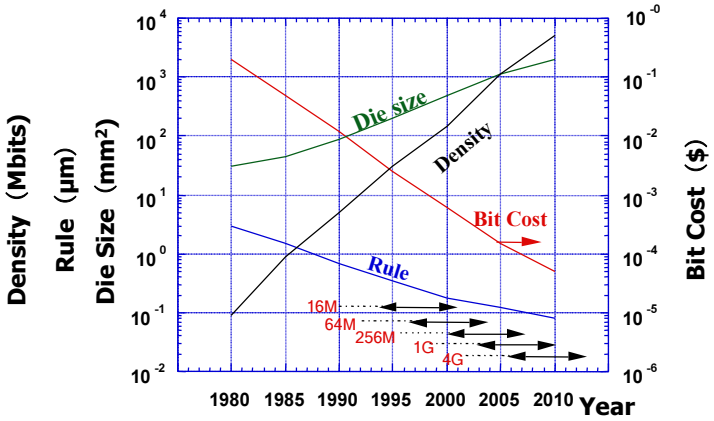
Bit Cost Trend of DRAMs



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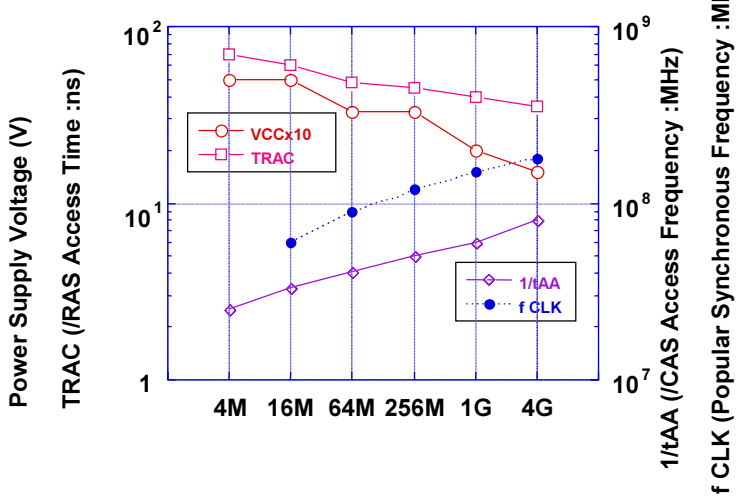
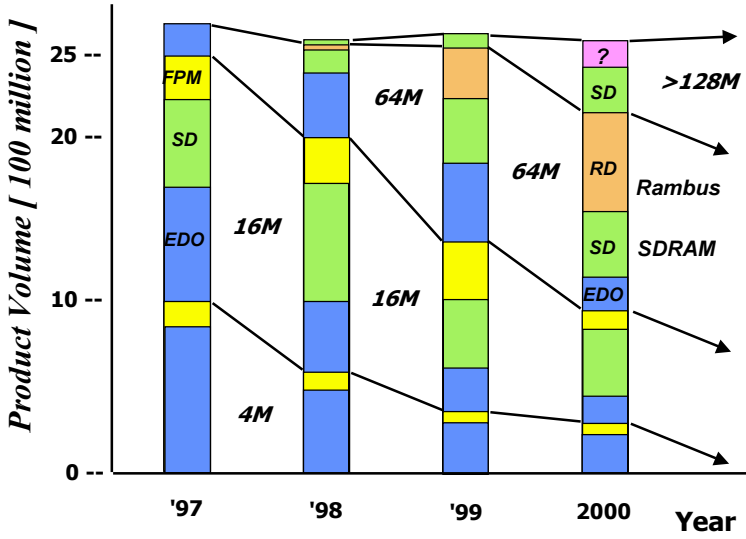
Access Time Trend



Standard DRAM Column Access Mode



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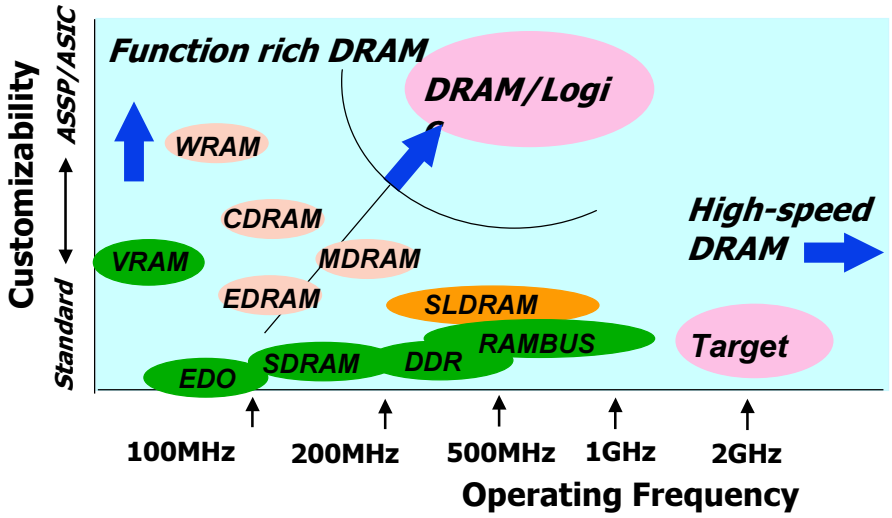
DRAM Operating Frequency v.s. Customizability



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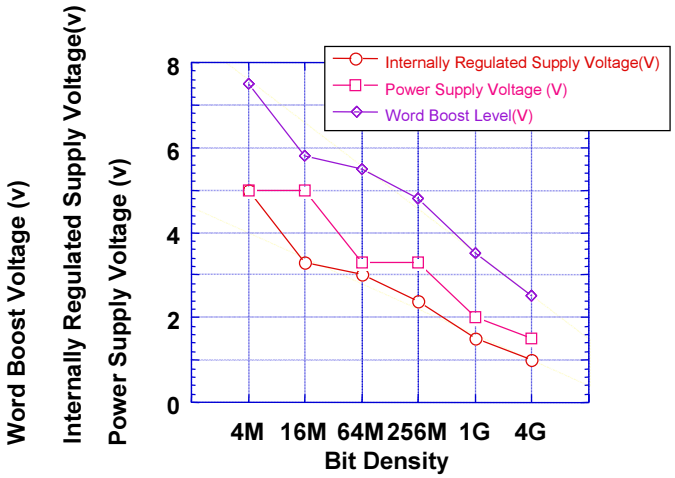
VCC & Vll & WL Voltage Trend



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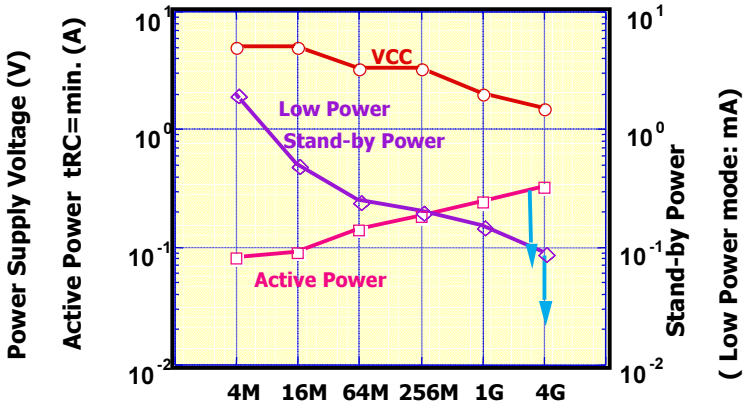
Power Dissipation Trend



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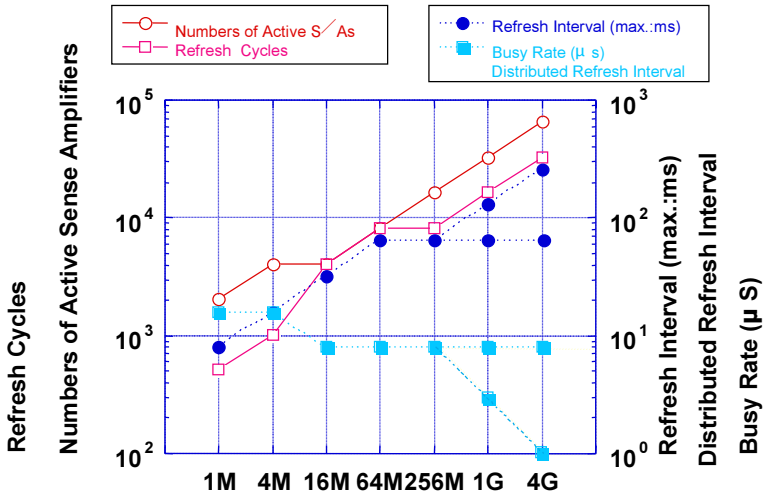
Refresh Specification Trend



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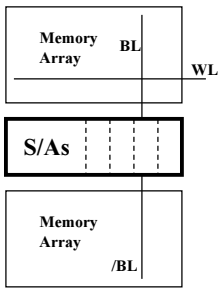
History

- *1K DRAM Intel 1103 introduced late 1971*
  - *-3Tr PMOS, 1P1M,*
  - *-Vdd=0v,Vss=16v,Vbb=20v, Trac=300ns*
- *4K DRAM TI TMS4030 introduced 1973*
  - *-1Tr NMOS, 1P1M, TTL I/O*
  - *-Vdd=12v,Vdd=5v, Vss=0v,Vbb=-3/-5v*
- *16K DRAM Mostek MK4116 introduced 1977*
  - *-1Tr NMOS, 2P1M, Address multiplex*
  - *-Vdd=12v,Vdd=5v, Vss=0v,Vbb=-5v, Trac=250ns*

***Open / Folded bit line, Double poly cell, Multi-PS*

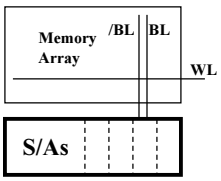
Bascic Bitline Structure (1)

Open Bitlines



Open BL
Cell Size $6F^2$
WL pitch: 3F
BL pitch: 2F

Folded Bitlines



Folded BL
Cell Size $8F^2$
WL pitch: 4F
BL pitch: 2F

Denser Memory
Uneven WL coupling

Relaxed S/A layout pitch
Even WL coupling

History (cont'd)

- 64K DRAM ('80,conference'79)
  - -Many changes at once - no dominant design
  - -Standardized, Page mode, Refresh functions
  - -Vcc=5v only,Vss=0v,Internal Vbb, Trac=200ns
  - -Boosted wordline, Active restore

- 256K DRAM ('83,conference'82)
  - -1Tr NMOS, 3P1M(FJ), I.I. mask increasing
  - -Vcc=5v only, Nibble/SC/CBR func., Trac=150ns
  - -Open v.s. Folded, Redundancy, CMOS prototype
  - -Vdd bitline pre-charge
  - -Some ASM, Wide I/O (x4)

History (cont'd)

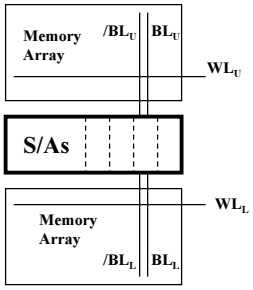
- 1M DRAM ('86,conference'84)
  - -N-well CMOS, 3P1M, Vdd/2 cell plate
  - -Half Vdd bitline reference and pre-charge,
  - -Shared folded bitline
  - -x4/x8, Package and module variety, Test circuits

- 4M DRAM ('89, conference'87)
  - -3D stacked or trench cell, CMOS, 4P1M,
  - -x16, Fast page/Self refresh, Trac=80ns
  - -Current-mirror data bus amp., Boosted I/O driver
  - -Word line strapping, Triple-well

DRAM Design Overview

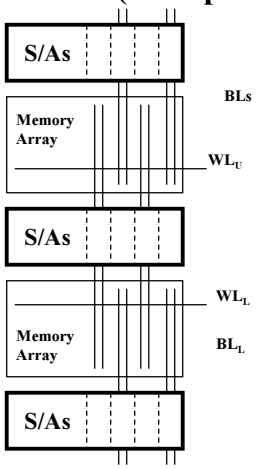
Basic Bitline Structure (2)

Folded Shared



Less area occupied by S/As

Interleaved (Multiplexed)



Used in nearly all 16M
Relaxes S/A pitch

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History (cont'd)

- *16M DRAM ('92, conference'90)*
  - *-N-well CMOS, 4P2M*
  - *-Internal Vdd down-converter (5v ext.---3.3v int.)*
  - *-Shared Y-decoder, Interleaved S/A,*
  - *-Vpp supply WL driver, RDRAM(PLL/DLL)*

- *64M DRAM ('95, conference '91)*
  - *-Triple well CMOS, Vss Substrate, 4P2M,*
  - *-Vdd=3.3v, Separate I/O PS-pin (Vddq/Vssq)*
  - *-SDRAM (clocked In, pipelined, burst I/O, term. I/F)*
  - *-COB, Staggered Sense amp.*

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Circuit Evolution Picking up

- 3Tr to 1Tr1C
- **Boosted Wordline**
- Single Power Supply (**Vbb gene., WL boost**)
- **Redundancy**
- **Vdd/2 BL pre-charge**
- **Internal DC converter**
- Clocked operation
- **PLL/DLL**
- **Multi-bank core**
- **Address Multiplex**
- **Open BL to Folded BL**
- NMOS to CMOS
- **Page & Refresh Mode**
- **Appli. Specific Circuits (ex. SR for VRAM)**
- **Test mode**
- Pipelined operation
- **High speed interface**
- Embedded core

Cell Array and Circuits

(1) 1 Transistor 1 Capacitor Cell

- ***Size Comparison to SRAM Cell***

(2) Array Example

(3) Major Circuits (today's example)

- ***Sense amplifier***
- ***Dynamic Row Decoder***
- ***Wordline Driver***

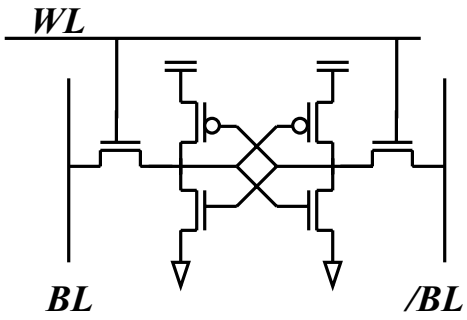
The other circuits interesting for VLSI designer

- ***Data bus amplifier***
- ***Reference generator***
- ***Replica technique***
- ***Voltage Regulator***
- ***Redundancy technique***
- ***High speed I/O circuits***

DRAM Design Overview

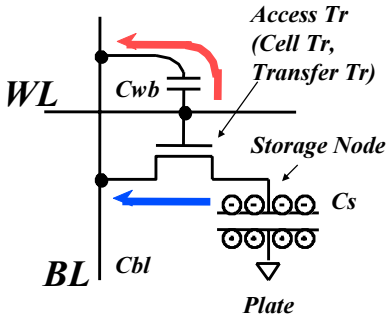
SRAM v.s. DRAM

6Tr embedded SRAM



Gain element in cell

1Tr1C Standard DRAM



Passive element
(No gain, Refresh needed)

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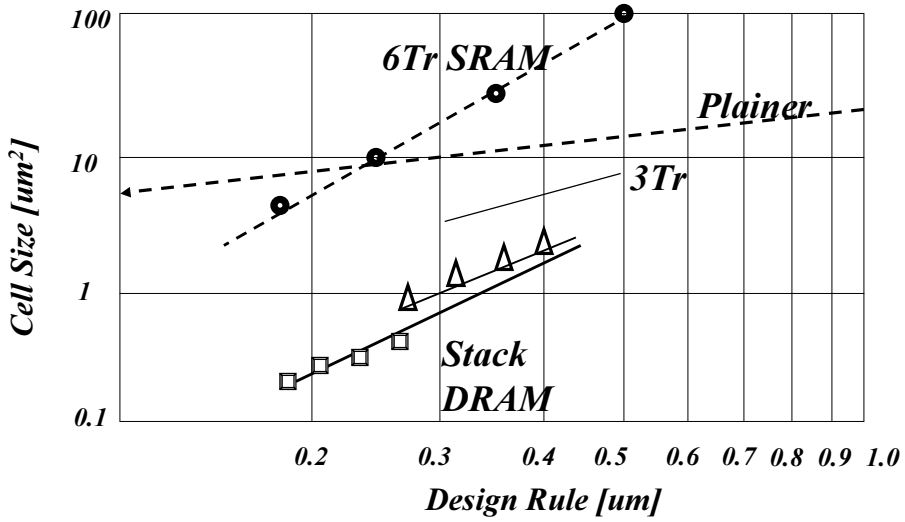
Comparison of SRAM and DRAM Cell Size



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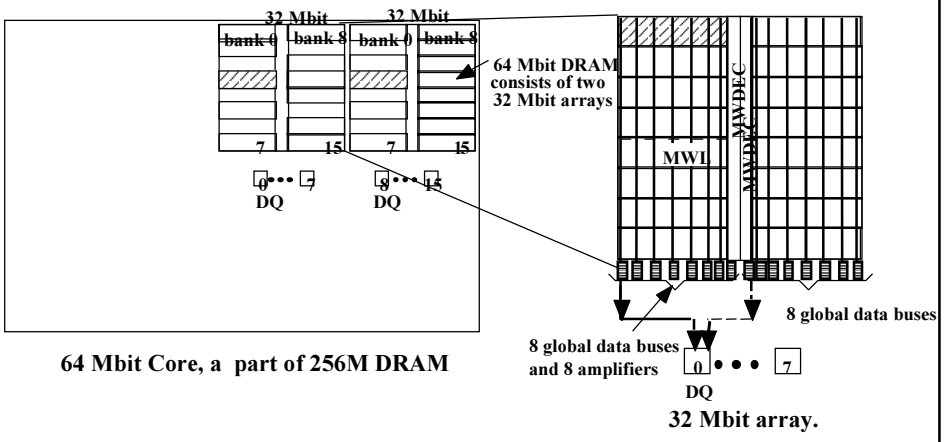
DRAM Design Overview

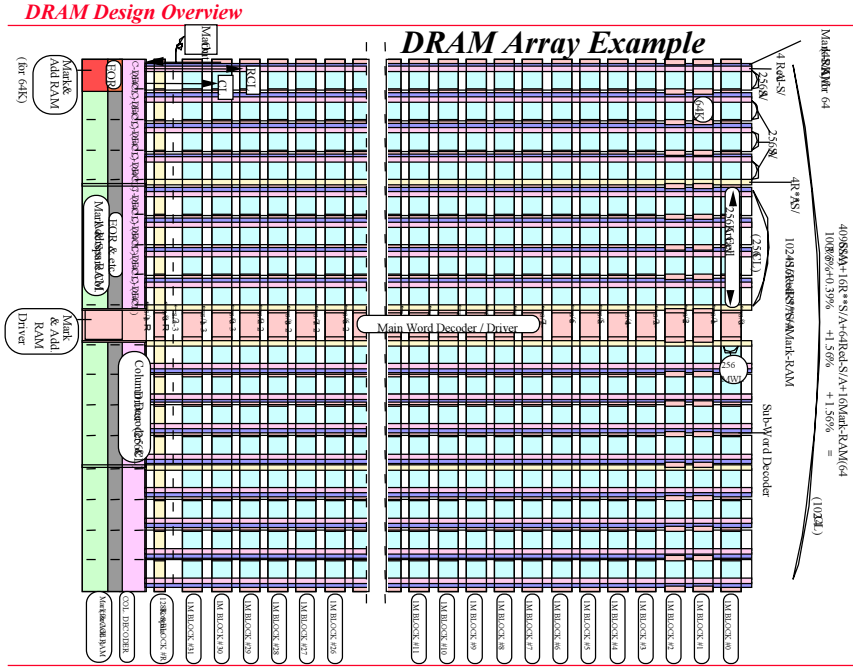
Standard DRAM Array Design Example



64 Mbit Core, a part of 256M DRAM

DRAM Design Overview

DRAM Array Example



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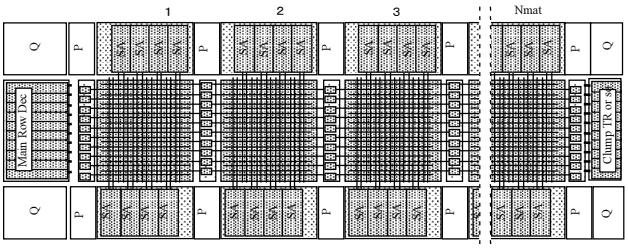
DRAM Array Example (cont'd)

Interleaved S／A & Hierarchical Row Decoder/Driver

(shared bit lines are not shown)



512K Array Nmat=16 or 12

(256 WL x 2048 SA)

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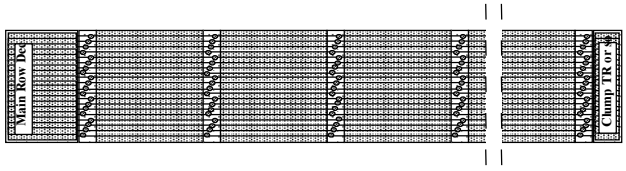
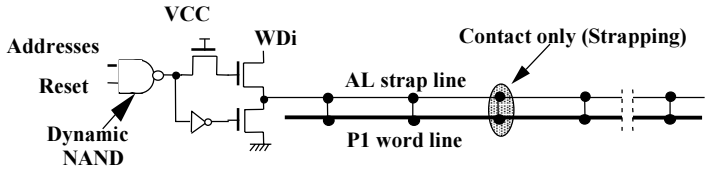
Row Decoder and Driver

＜WL Strapping Type＞





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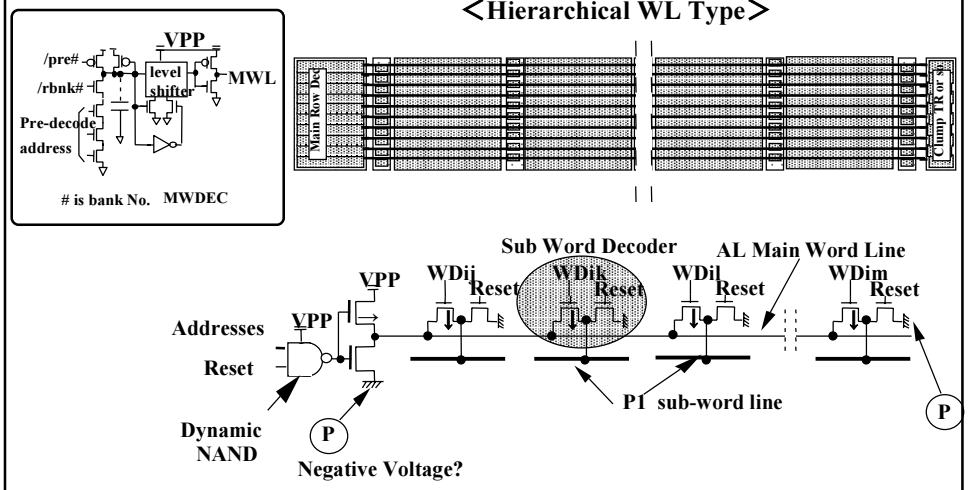
Row Decoder and Driver (cont'd)



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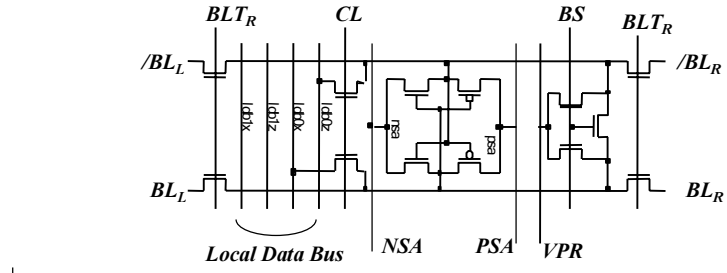
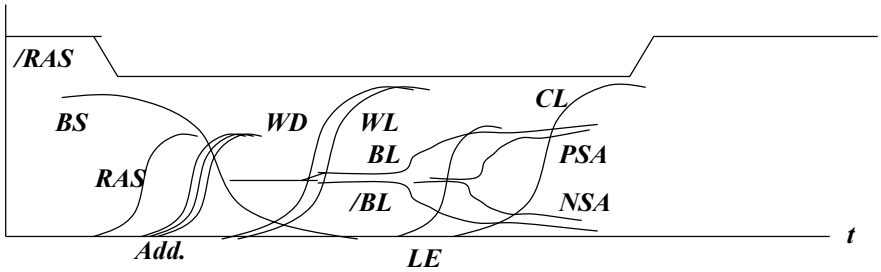
DRAM Design Overview

Sense Amplifier Circuits - Folded Shared Interleaved -





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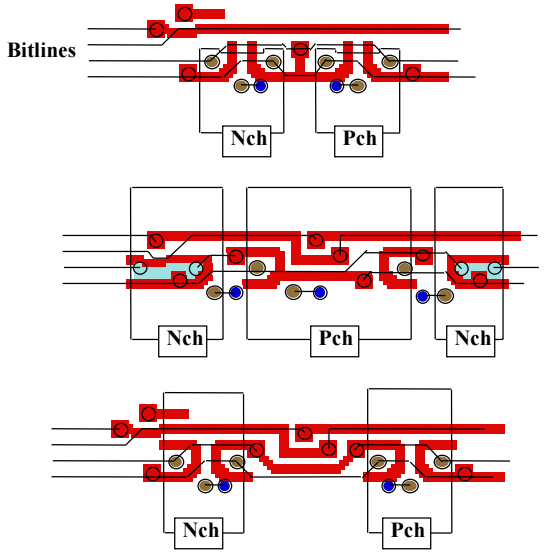
Sense Amplifier Pitch Matched Layout



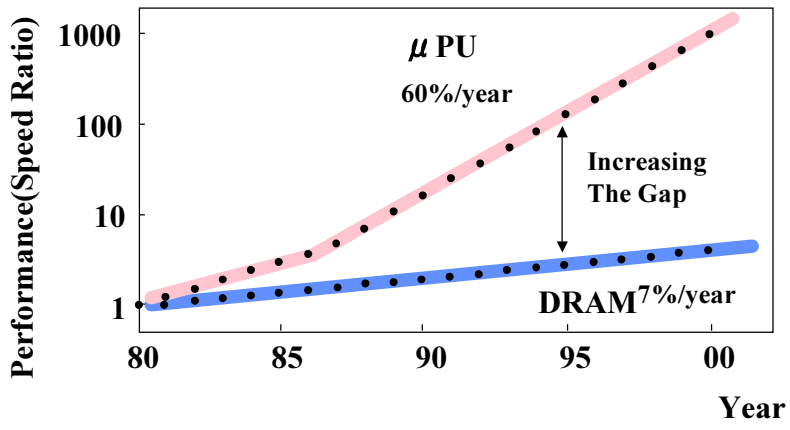
Standard DRAM Design Feature

- *Tightly depends on technology*
- *The row circuits is fully different from SRAM.*
- *Few product variation in the same technology*
- *"Trends" is mother , "Cost" is father .*
- *"Standard" gives us less freedom!*
- *Almost always analogue circuit design*
- *Simply forward critical path*
- *CAD: Spice-like circuits simulator*
  Fully handcraft layout,
  Whole-chip tools must be a dream.

Embedded DRAM or Merged D&L

- *Merged DRAM and Logic*
  - *-Technology choice and cost issue*
    - *----People have talked too much above.*
  - *-Otherwise, that's a near future evolution.*
- *Current Technology behind advanced DRAMs'*
- *Small ASIC seems to be not yet on the business.*
- *How solve the following technical problem?*
  - *memory wall, granularity, I/O power*

Speed Gap between DRAM and CPU - Memory Wall -



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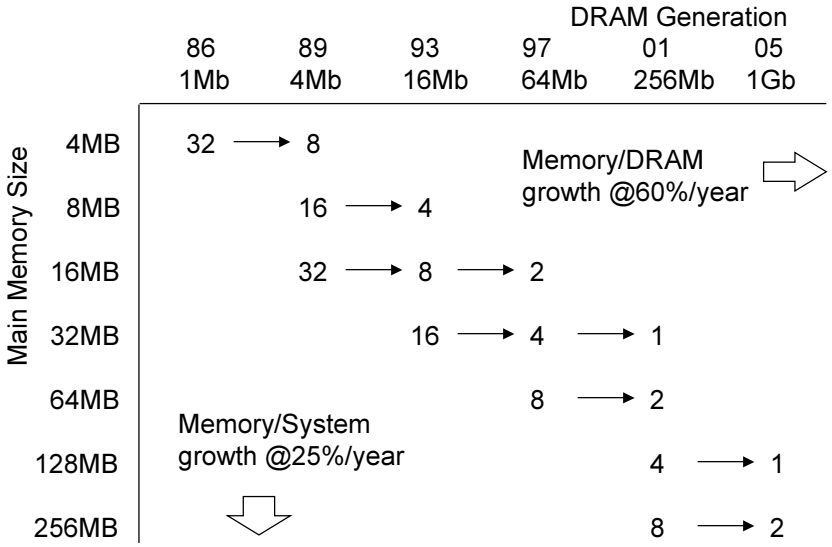
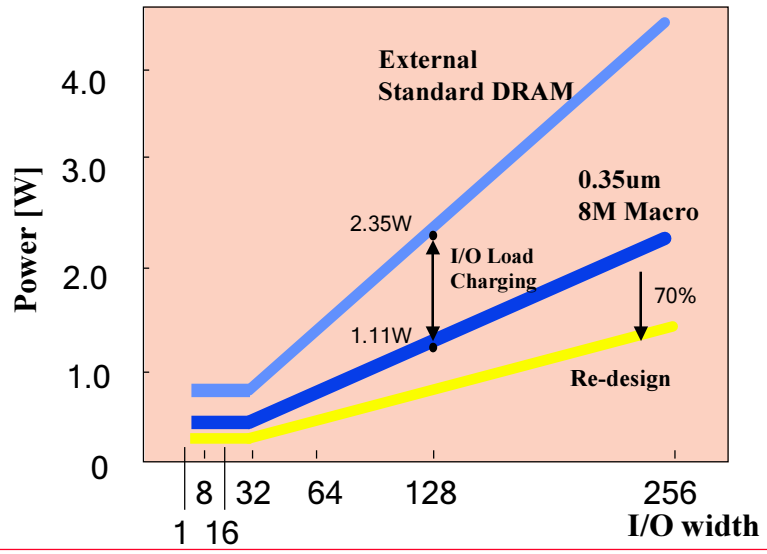
The numbers of DRAM on PCs



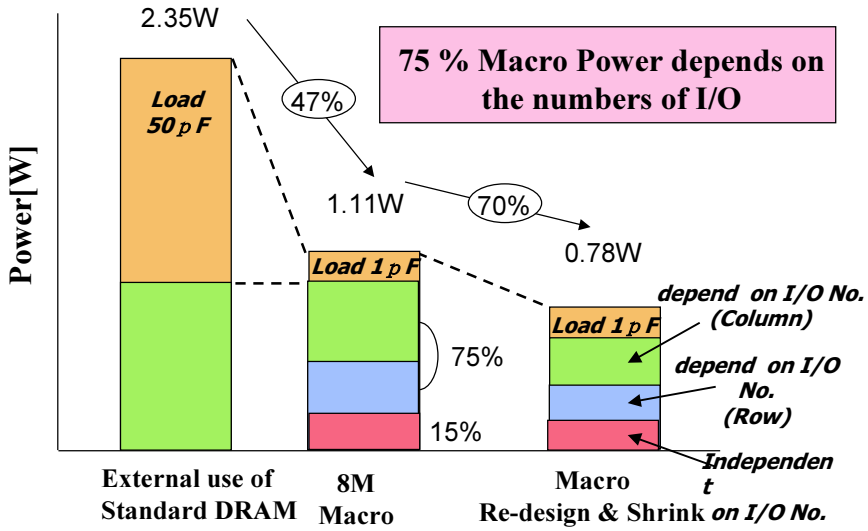
DRAM Design Overview

Macro Power (MDL v.s. Standard DRAM)



DRAM Design Overview

Macro Power (cont'd)



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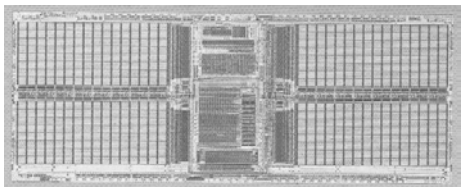
The First Commercial Product of Embedded DRAM



M32R/D (Mitsubishi)

- **0.45μm DRAM**
- **32-bit RISC CPU + 16Mbit DRAM**
- **Die Size: 153.7mm^2**

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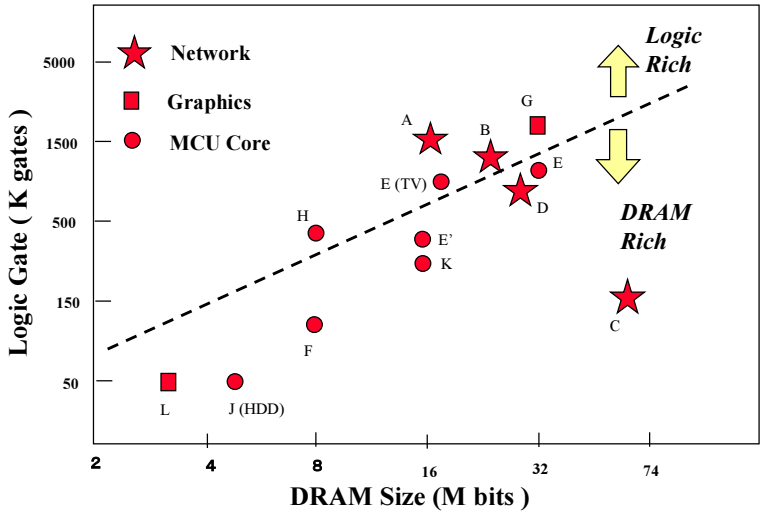
DRAM Design Overview

0.25um Embedded DRAM Products

DRAM v.s. Logic Size



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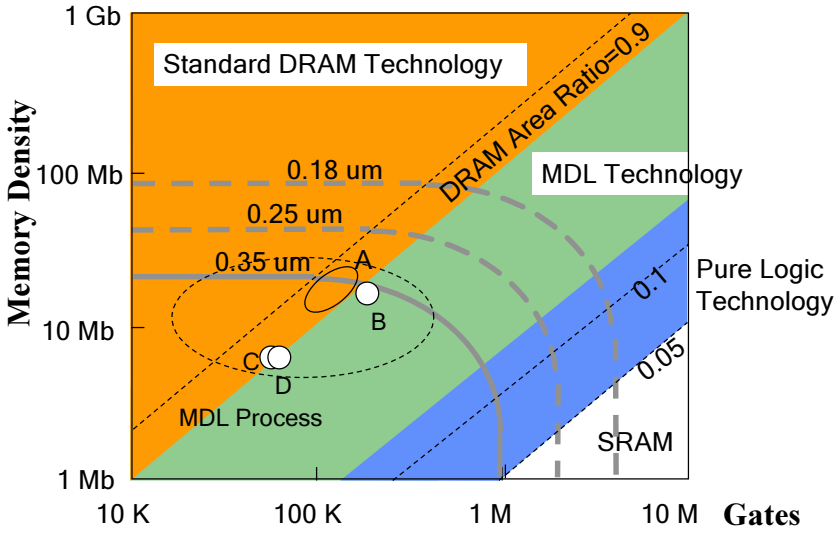
DRAM Design Overview

Memory Density and Logic Gates

: Affordable DRAM-density & Logic-gates in a 100mm² Die



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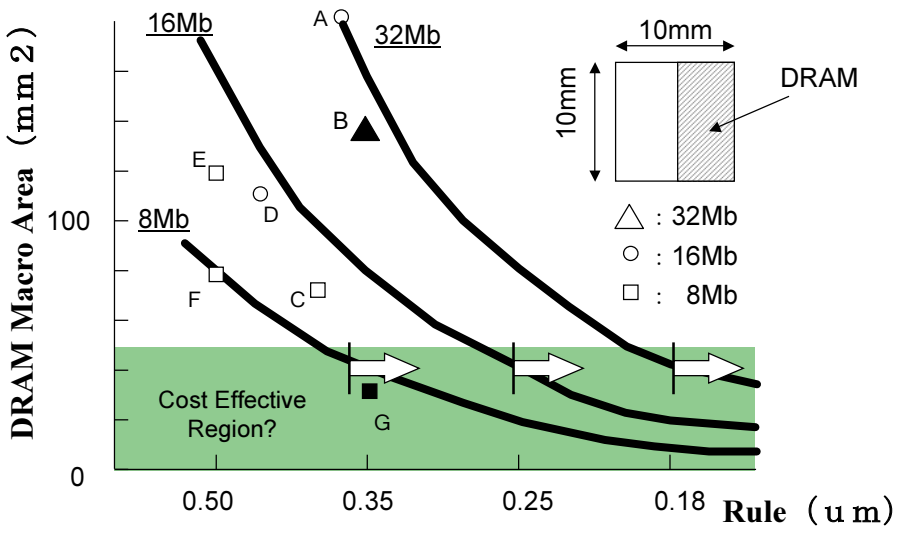
DRAM Macro Size Shrink
— Which could make cost effective ?



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DRAM Design Overview

Application Specific Memory

-Brief Introduction-

- ***Various ASM introduced since '83***
  - ***-VRAM: 64K to 4M VRAM***
  - ***-Field Memory(NEC), Triple Port(FJ)***
  - ***-mostly for ASICs or conference chips***
- ***Only VRAM got a semi-standardization***
- ***Longer design TAT***
  - ***as more complicated spec. and circuits***
- ***Redundancy and Test isuues: big problems***
- ***Never major products***

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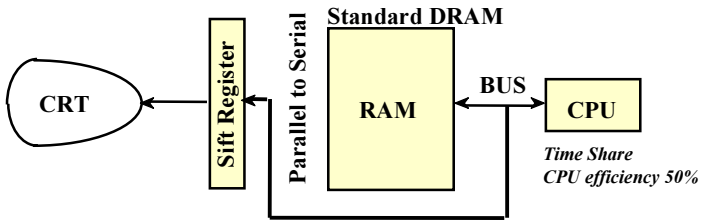
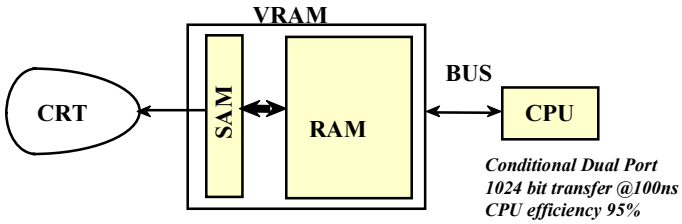
DRAM Design Overview

256K Dual Port Video RAM



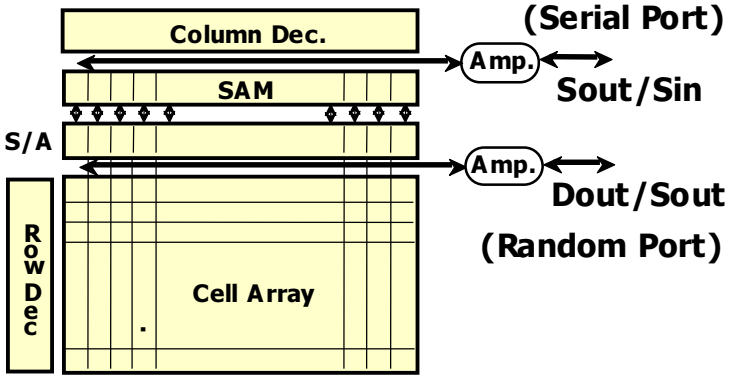
(a) Conventional 2D Graphic System



(b) 2D Graphic System used VRAM

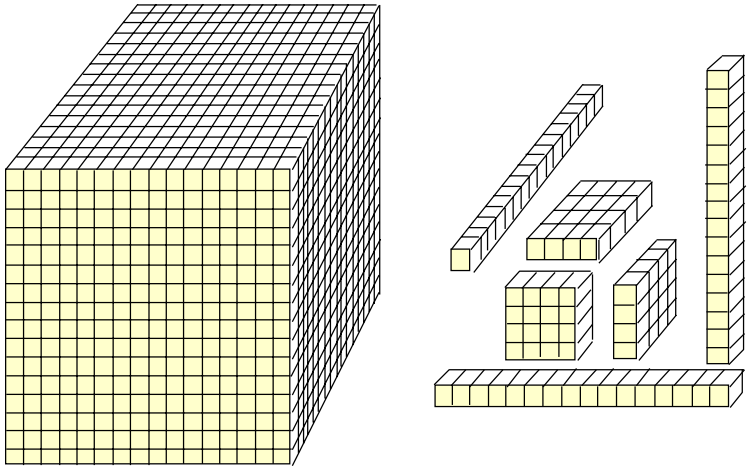
DRAM Design Overview

256K Dual Port Video RAM (cont'd)



- *Narrow pitch matched SAM (or Sift Register) design*
- *No explicit bus for a mass of data transfer at a time*
- *A hinted solution by utilizing a memory parallelism*

4M bit Cubic Memory (conference '90)



- *16b x 16b x 16b (4Kbit) virtual bit map space*
- *six different ways of column access on the fly access*

Summary

- *Passive 1Tr1C cell leads all the features of dynamic circuits and design complexity.*
- *The row circuits is fully different from SRAM.*

- *A Dinosaur, Standard DRAM, become almost dead, because of both the technology saturation and the narrow band-width itself.*

- *The design technique should be transferred for the coming embedded era.*